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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,853	12/02/2003	Scott Fairbanks	6429P001	5587

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EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,853	FAIRBANKS, SCOTT	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-44 and 46-76* is/are rejected.

7)☒ Claim(s) *45* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *23 May 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Applicant's Argument

1. Applicant's response letter received on 5/23/2005 has been received and entered in the case. Applicant's arguments with respect to the prior art rejections mailed on 01/13/2005 have been fully considered and found persuasive, as such; the prior art rejections have been withdrawn. A new action on the merits appears below.

2. As to the objection to the drawings, Applicant's clarification has overcome the objection, as such; the objection has been withdrawn.

Claim Objections

3. Claim 56 is objected to because of the following informalities: in line 1, "apparatus" should be changed to --integrated circuit--; and in line 2, "an" should be changed to --the--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) The invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 2, 4-7, 10-12, 14-22, 24-31, 33-40, 42-44, 46-53, 55-73, 75 and 76 are rejected under 35 U.S.C. 102(a) as being anticipated by Moore et al., The Distributed Clock Generator (6

pages) by Simon Moore & Scott Fairbanks, Computer Laboratory, University of Cambridge, UK December 5, 2001 (I.D.S.).

With regard to claim 1, Moore et al. discloses in Fig. 4 an apparatus comprising a clock generator, distributed over an integrated circuit, including a plurality of cells each coupled to multiple adjacent ones of the plurality of cells by different clock wires, wherein, for each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge.

With regard to claims 2, 4-7, and 10, the reference also meets the recited limitations in these claims.

With regard to claim 11, Moore et al. discloses in Fig. 4 an apparatus comprising a clock generator to generate a clock signal through the interaction of a plurality of cells distributed in grid over an integrated circuit, wherein each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires; and an inherent plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein the plurality of sets of synchronous logic are interconnected.

With regard to claims 12 and 14-20, the reference also meets the recited limitations in these claims.

With regard to claim 21, Moore et al. disclose in Fig. 4 an integrated circuit including a clock generator including a plurality of cells distributed in grid over an integrated circuit that collectively form an oscillator of the clock generator, wherein each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells;

and an inherent plurality of sets of synchronous logic, distributed over the integrated circuit, coupled to be clocked by the clock generator.

With regard to claims 22 and 24-29, the reference also meets the recited limitations in these claims (see Fig. 4 of Moore et al.).

With regard to claim 30, Moore et al. discloses in Fig. 4 an integrated circuit comprising a distributed clock generator including, a plurality of cells that, responsive to an averaging of a previous clock edge produced by the plurality of cells, detect when to produce the next clock edge, and a plurality of clock wires each coupling together two of the plurality of cells such that the plurality of cells are coupled together in grid; and an inherent plurality of sets state holding elements each having a clock input, each clock input of each of the sets coupled to a different one of the plurality of clock wires.

With regard to claims 31 and 33-38, the reference also meets the recited limitations in these claims (see Fig. 4 of Moore et al.).

With regard to claims 39 and 75, Moore et al. discloses in Fig. 4 a distributed clock generator, and a method of use thereof, comprising a plurality of cells each including, a plurality of terminals, a cumulative clock edge detection circuit coupled to the plurality of terminals and having an output, a delay/amplification circuit coupled to the output of the cumulative clock edge detection circuit, and a driver circuit coupled to the plurality of terminals and to the delay/amplification circuit; a plurality of clock wires, each of the plurality of clock wires coupling one of the plurality of terminals of one of the plurality of cells to one of the plurality of terminals of another of the plurality of cells.

With regard to claims 40, 42-44, 46-51, and 76 the reference also meets the recited limitations in these claims (see Fig. 4 of Moore et al.).

With regard to claim 52, Moore et al. discloses in Fig. 4 an integrated circuit comprising a distributed clock generator including a plurality of cells collectively having a plurality of terminal pairs, each of the plurality of terminal pairs including a charging terminal coupled to a discharging terminal to have generated there between a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal, the terminals of each of the plurality of terminal pairs being part of two different ones of the plurality of cells, the plurality of cells coupled together as a result of each being coupled to certain others of the plurality of cells by the plurality of terminal pairs; and an inherent plurality of sets of synchronous logic each having a clock input, each clock input of each of the sets coupled to receive the clock signal of one of the plurality of terminal pairs.

With regard to claims 53 and 55-61 the reference also meets the recited limitations in these claims (see Fig. 4 of Moore et al.).

With regard to claim 62, Moore et al. discloses in Fig. 4 a cell of a distributed clock generator comprising: a set of terminals of the cell, each of the terminals in the set being one terminal of a different terminal pair, each of the terminal pairs including a charging terminal coupled to a discharging terminal to have generated there between a clock signal having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal; a cumulative clock edge detection circuit coupled to the set of terminals to determine a single clock edge transition time reflective of transitions of the clock signals on the terminals, a driver circuit coupled to the set of terminals; and a delay/amplification circuit, coupled to an

output of the cumulative clock edge detection circuit and to the driver circuit, to cause another clock edge transition of the clock signals to substantially simultaneously occur some delay time after each of the single clock edge transition times.

With regard to claims 63-73 the reference also meets the recited limitations in these claims (see Fig. 4 of Moore et al.).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 13, 23, 32, 41, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. in view of Graef (US 6,305,001; previously cited).

With regard to claim 3, the above discussed clock generator circuit of Moore et al. meets all of the claimed limitations except that Moore et al. does not disclose that the clock grid is three-dimensional. Graef teaches a similar clock generator circuit having three-dimensional grid (see column 13, lines 17-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Graef with the prior art by implementing the clock grid in three-dimensional in order to minimize chip area.

Claims 13, 23, 32, 41, and 54 are similarly rejected; note the above discussion with regard to claim 3.

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al.

The above-discussed clock generator circuit of Moore et al. meets all of the claimed limitations except that the shape is not specifically mentioned, such as irregular shape or one of a square and a rectangle. However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to change the shape of the clock grid circuit for meeting specific condition which is in each case optimally matched to its application. Since it has been held that discovering an optimum skill in the art. See *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

9. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. in view of Kondoh et al. (US 5,883,534).

The above-discussed clock generator circuit of Moore et al. meets all of the claimed limitations except that the delay time is using a single inverter as a delay element instead of a plurality of variable delay inverters. Kondoh et al. teaches in Fig. 5 a delay circuit having a plurality of variable delay inverters. Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to replace the delay element in the circuit of the prior art with the delay as taught by Kondoh et al. in order to meet the specific timing condition of the particular application.

Allowable Subject Matter

10. Claim 45 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Fig. 7), as recited in claim 45, having specific structural limitations such as each of the plurality of cells is a hybrid type cell (701-716, which is also shown in detailed as 600 in instant Fig. 6) in which each driver circuit includes at least one pull-up driver (609, 611) and at least one pull-down driver (610, 612) coupled to different ones of the plurality of terminals, and wherein the plurality of clock wires couple together the terminals coupled to pull-up drivers and pull-down drivers; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

Conclusion

11. In view of the new grounds of rejection, this action is non-final.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
June 13, 2005

Kenneth B. Wells
Primary Examiner